Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device having an input/output protection circuit section on a semiconductor substrate, the input/output protection circuit section comprising:

a plurality of field effect transistors connected in parallel, each of which has a source diffusion layer of a first conductive type and a drain diffusion layer of the first conductive type, a channel region therebetween and a gate electrode that is disposed between said source and drain diffusion layers;

a dopant diffusion region of a second conductive type that is set at a distance from said plurality of field effect transistors; and

an element isolation film located in the substrate between the dopant diffusion region of the second conductive type and the source diffusion layer of the first conductive type, for separating the dopant diffusion region from the source diffusion layer,

wherein said dopant diffusion region is connected to a reference potential, and wherein the source diffusion layer is also connected to said reference potential,

wherein the drain diffusion layer is connected directly to an input/output terminal section without an intervening resistance element,

wherein a first conductive type well having a lower dopant concentration than the dopant concentration of the source diffusion layer is formed directly under the source diffusion layer and thereby the first conductive type well is electrically connected directly with the source diffusion layer, wherein no first conductive type well is formed under or electrically connected to the drain diffusion layer,

wherein the first conductive type well at least partially underlies the element isolation film, and

wherein a second conductive type well is formed on the surface of the semiconductor substrate, said source and drain diffusion layers of the first conductive type and said dopant diffusion region of the second conductive type are disposed over the second conductive type well, and thereby the dopant diffusion region of the second conductive type is electrically connected directly with the second conductive well, but the first conductive well is not physically contacted directly with the dopant diffusion region of the second conductive type.

~~wherein said source and drain diffusion layers each have an extension region extending into said channel region, said source extension region not extending between said source diffusion layer and said first conductive type well, said source and drain extension regions each having a dopant concentration between the dopant concentration of said source and drain diffusion layers and the dopant concentration of said first conductive type well.~~

2. (Cancelled)

3. (Previously Presented) The semiconductor device claimed in Claim 1, wherein said plurality of field effect transistors are N-channel type field effect transistors, and wherein said source diffusion layer is also connected to the reference potential to which said dopant diffusion region is connected.

4. (Currently Amended) A semiconductor device having an input/output protection circuit section on a semiconductor substrate, the input/output protection circuit section comprising:

a complementary field effect transistor including a first field effect transistor having a source diffusion layer of a first conductive type, a drain diffusion layer of the first conductive type, a channel region therebetween and a gate electrode that is disposed between the source and drain diffusion layers of the first conductive type, and a second field effect transistor having a source diffusion layer of a second conductive type, a drain diffusion layer of the second conductive type, and a gate electrode that is disposed between the source and drain diffusion layers of the second conductive type,

wherein a first dopant diffusion region of the second conductive type is set at a distance from said first field effect transistor, and a second dopant diffusion region of the first conductive type is set at a distance from said second field effect transistor,

wherein at least an element isolation film is located in the substrate between the first dopant diffusion region of the second conductive type and the source diffusion layer of the first conductive type, for separating the first dopant diffusion regions from the source diffusion layer of said first field effect transistor,

wherein the first dopant diffusion region is connected to a first reference potential, the source diffusion layer of the first field effect transistor is also connected to the first reference potential, ~~and~~ the second dopant diffusion region is connected to a second reference potential, and the source diffusion layer of the second field effect transistor is also connected to the second reference potential,

wherein the drain diffusion layer of the first field effect transistor and the drain diffusion layer of the second field effect transistor are each connected directly to an input/output terminal section without an intervening resistance element,

wherein a first conductive type well having a lower dopant concentration than dopant concentration of the source diffusion layer of the first field effect transistor is formed directly under the source diffusion layer of the first field effect transistor and thereby the first conductive type well is electrically connected directly with the source diffusion layer of the first filed effect transistor, wherein no first conductive type well is formed under the drain diffusion layer of the first field effect transistor or is electrically connected with the drain diffusion layer of the first field effect transistor,

wherein the first conductive type well of the first field transistor at least partially underlies the element isolation film of the first field effect transistor, and

wherein a second conductive type well is formed on the surface of the semiconductor substrate of the first field effect transistor, said source and drain diffusion layers of the first conductive type and said dopant diffusion region of the second conductive type are disposed

over the second conductive type well, and thereby the dopant diffusion region of the second conductive type for the first field effect transistor is electrically connected directly with the second conductive type well, but the first conductive well is not physically contacted directly with the dopant diffusion region of the second conductive type.

~~wherein said source and drain diffusion layers of said first conductivity type each have an extension region extending into said channel, said source extension region not extending between said source diffusion layer and said first conductive type well, said source and drain extension regions each having a dopant concentration between the dopant concentration of said source and drain diffusion layers of said first conductive type and the dopant concentration of said first conductive type well.~~

5. (Previously Presented) The semiconductor device claimed in Claim 4,

wherein the gate electrode, the source and drain diffusion layer of the first conductive type and the first dopant diffusion region of the second conductive type of the first field effect transistor are disposed over a second conductive type well that is formed on the surface of the semiconductor substrate, and

wherein the bottom of said first conductive type well of the first field effect transistor is formed at the same depth as the bottom of the second conductive type well of the first field effect transistor or at a level deeper than the bottom of the second conductive type well.

6. (Previously Presented) The semiconductor device claimed in Claim 5,

wherein, beneath the second conductive type well of the first field effect transistor, there is set a dopant high-concentration region containing second conductive type dopants with a higher dopant concentration than the second conductive type well of the first field effect transistor, and

wherein the bottom of said first conductive type well of the first field effect transistor is formed at the same depth as the bottom of said dopant high-concentration region or at a level deeper than the bottom of said dopant high-concentration region.

7. (Previously Presented) The semiconductor device claimed in Claim 4, wherein the first field effect transistor is an N-channel type field effect transistor, and

wherein the source diffusion layer of the first field effect transistor is also connected to the first reference potential, to which said first dopant diffusion region is connected.

8. (Currently Amended) A semiconductor device having an input/output protection circuit section on a semiconductor substrate, the input/output protection circuit section comprising:

a plurality of field effect transistors connected in parallel, each of which has a source diffusion layer of a first conductive type and a drain diffusion layer of the first conductive type, a channel region therebetween and a gate electrode that is disposed between said source and drain diffusion layers;

a dopant diffusion region of a second conductive type that is set at a distance from said plurality of field effect transistors; and

an element isolation film located in the substrate between the dopant diffusion regions of the second conductive type and the source diffusion layer of the first conductive type, for separating the dopant diffusion regions from the source diffusion layer,

wherein said dopant diffusion region and said source diffusion layer of the first conductive type are connected to a reference potential,

wherein the drain diffusion layer is connected directly to an input/output terminal section without an intervening resistance element,

wherein a first conductive type well with a lower dopant concentration than the dopant concentration of the source diffusion layer is formed directly under the source diffusion layer and thereby the first conductive type well is electrically connected directly with the source diffusion layer of the first conductive type, wherein no first conductive well is formed under or electrically connected to the drain diffusion layer of the first conductive type,

wherein the first conductive type well at least partially underlies an element isolation film ~~separating the source diffusion layer from the dopant diffusion region of the second conductive type~~, and

wherein a second conductive type well is formed on the surface of the semiconductor substrate, the source and drain diffusion layers of the first conductive type and the dopant diffusion region of the second conductive type are disposed over the second conductive well, and thereby the dopant diffusion region of the second conductive type is electrically connected directly with the second conductive well, but the first conductive well is not physically contacted directly with the dopant diffusion region of the second conductive type.

~~wherein said source and drain diffusion layers each have an extension region extending into said channel region, said soruce extension region not extending between said source diffusion layer and said first conductive type well, said source and drain extension regions each having a dopant concentration between the dopant concentration of said source and drain diffusion layers and the dopant concentration of said first conductive type well.~~

9. (Cancelled)

10. (Previously Presented) A semiconductor device claimed in Claim 1, wherein the source diffusion layer is connected to a ground terminal.

11. (Currently Amended) A semiconductor device having an input/output protection circuit section on a semiconductor substrate, the input/output protection circuit section comprising:

a plurality of field effect transistors connected in parallel, each of which has a source diffusion layer of a first conductive type and a drain diffusion layer of the first conductive type, a channel region therebetween and a gate electrode that is disposed between said source and drain diffusion layers;

a dopant diffusion region of a second conductive type that is set at a distance from said plurality of field effect transistors; and

an element isolation film located in the substrate between the dopant diffusion region of the second conductive type and the source diffusion layer of the first conductive type, for separating the dopant diffusion region from the source diffusion layer,

wherein said dopant diffusion region is connected to a reference potential, and the source diffusion layer is also connected to the reference potential,

wherein the drain diffusion layer is connected directly to an input/output terminal section without an intervening resistance element,

wherein a first conductive type well with lower dopant concentration than the dopant concentration of the source diffusion layer is formed directly under the source diffusion layer and thereby the first conductive type well is electrically connected directly with the source diffusion layer, wherein no first conductive type well is formed under the drain diffusion layer or is electrically connected with the drain diffusion layer,

wherein the first conductive type well at least partially underlies the element isolation film, and

wherein a second conductive type well is formed on the surface of the semiconductor substrate, said source and drain diffusion layers of the first conductive type and said dopant diffusion region of the second conductive type are disposed over the second conductive well, and thereby the dopant diffusion region of the second conductive type is electrically connected directly to the second conductive type well, but the first conductive well is not physically contacted directly with the dopant diffusion region of the second conductive type,

~~wherein the gate electrode, the source and drain diffusion layers of the first conductive type and the dopant diffusion region of the second conductive type are disposed over the second conductive type well that is formed on the surface of the semiconductor substrate,~~

wherein the bottom of said first conductive type well is formed at the same depth as the bottom of the second conductive type well or at a level deeper than the bottom of the second conductive type well; and

wherein said source and drain diffusion layers are both made to have an extension region that is set at end sections of the source diffusion layer and the drain diffusion layer on the side of the channel region, and the dopant concentration of the extension region is lower than the dopant concentration of said source and drain diffusion layers, but higher than the dopant concentration of the first conductive well.

~~wherein said source and drain diffusion layers each have an extension region extending into said channel region, said source extension region not extending between said source diffusion layer and said first conductive type well, said source and drain extension regions each having a dopant concentration between the dopant concentration of said source and drain diffusion layers and the dopant concentration of said first conductive type well.~~

12. (New) The semiconductor device claimed in Claim 1,

wherein each of said field effect transistors has a gate length or a length of the gate electrode not greater than 0.2 μm.

13. (New) The semiconductor device claimed in Claim 1,

wherein each of said field effect transistors has a gate length or a length of the gate electrode not greater than 0.2 μm; or the source diffusion layer and the drain diffusion layer are both made to have an extension region that is set at end sections of the source diffusion layer and the drain diffusion layer on the side of the channel region, and wherein the dopant concentration of the extension region is lower than the dopant concentration of said source and drain diffusion layers but higher than the dopant concentration of the first conductive type well.

14. (New) The semiconductor device claimed in Claim 4,

wherein each of said field effect transistors has a gate length or a length of the gate electrode not greater than 0.2 μm.

15. (New) The semiconductor device claimed in Claim 4,

wherein said first field effect transistor has an addition arrangement that the source region and the drain diffusion layer of the first field effect transistor are both made to have an extension region that is set at end sections of said source diffusion layer and said drain diffusion layer on the side of the channel region of the first field effect transistor, and wherein the dopant concentration of the extension region is lower than the dopant concentration of said source and drain diffusion layers but higher than the dopant concentration of the first conductive type well.

16. (New) The semiconductor device claimed in Claim 8,

wherein each of said field effect transistors has a gate length or a length of the gate electrode not greater than 0.2 μm.

17. (New) The semiconductor device claimed in Claim 8,

wherein each of said field effect transistors has an addition arrangement that the source region and the drain diffusion layer are both made to have an extension region that is set at end sections of said source diffusion layer and said drain diffusion layer on the side of the channel region, and wherein the dopant concentration of the extension region is lower than the dopant concentration of said source and drain diffusion layers but higher than the dopant concentration of the first conductive type well.